CMOS IMAGE SENSOR AND METHOD FOR SENSING AN IMAGE USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application relies for priority upon Korean Patent Application No. 2003-58463 filed on August 23, 2003, the contents of which are herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to a CMOS (Complementary Metal Oxide Silicon) image sensor and a method for sensing an image using the same.

2. Description of the Related Art

[0003] A photo detector detects light, converts the detected light into an electrical signal, and outputs an image signal. For example, the photo detector may be included in a CCD (Charge Coupled Device) or a CMOS image sensor.

[0004] The CCD includes a light-sensitive element such as a photo diode, a charge transmission element and a signal output element. The photo diode detects light and generates a charge signal (or a photo charge) that is indicative of the amount of light received by the photo diode. The charge transmission element transmits the charge signal generated from the photo diode without signal loss to the signal output element. The signal output

element accumulates the charge signal, and outputs an analog voltage signal in proportion to the quantity of the charge signal.

[0005] The CCD sequentially transmits the charge signal to neighboring pixels, but does not randomly access the pixels.

[0006] A CMOS image sensor has a few advantages over the CCD. In particular, the fabrication process of the CMOS image sensor is simpler than that of the CCD. In addition the CMOS image sensor employs a correlated double sampling circuit to greatly reduce a reset noise caused by resetting the charges accumulated from the photo diodes.

[0007] The correlated double sampling circuit samples a reset voltage of a pixel, and then samples a signal voltage. An output of the correlated double sampling circuit equals the difference between the reset voltage and the signal voltage. Thus, the correlated double sampling circuit may reduce fixed pattern noises due to threshold voltage differences of the transistors in pixels, and the correlated double sampling circuit reduces the reset noise due to the reset voltage differences.

One example of a pixel in the CMOS image sensor has a photo diode and four transistors. The four transistors function to transfer charge from the photo diode to the correlated double sampling circuit and to reset the accumulated charge. FIG. 1 illustrates an example of a CMOS image sensor having a photo diode and four transistor structure. As shown, a plurality of row lines 115 cross a plurality of column lines 113. At respective crossing, pixels 101 having a photo diode and four transistor structure are formed. As

further shown, reset lines 117provide reset signals Rs for causing the pixels 101 to reset their charges, and selection lines 119 provide selection signals RSEL for causing pixels to transfer charges to an associated column line 113.

[0009] The CMOS image sensor having pixels of the four-transistor structure has an advantage that noise is reduced, but has a disadvantage that the fill factor of the pixel is low. In other words, the area occupied by the photo diode in one pixel is relatively reduced since the pixel includes four transistors. An increased number of pixels and a decreased area occupied by a unit pixel may lead to a CMOS image sensor of high resolution. A low fill factor leads to a decrease in the area occupied by the photo diode. This decreased area occupied by the photo diode reduces the quantity of the electron-hole pairs generated by light incident on the photo diode, and thus the quantum efficiency (Q.E.) of the CMOS image sensor decreases. Therefore, the decreased quantum efficiency of the CMOS image sensor deteriorates the sensitivity of the CMOS image sensor.

SUMMARY OF THE INVENTION

[0010] The present invention provides an image sensor and method of image sensing.

[0011] In an exemplary embodiment, the pixels of the image sensor have a reduced number of transistors. This has the advantage of providing for an increased fill factor.

[0012] In another exemplary embodiment, column lines of the image sensor receive the charges generated by the pixels, and a reset circuit is associated with each column line. Each reset circuit is configured to reset the charges generated by the pixels associated with the same column line. Accordingly, a reset operation may be performed while maintaining a reduced number of transistors in an individual pixel. This promotes an increased fill factor and/or greater pixel density.

[0013] In one exemplary embodiment, the image senor includes a plurality of row lines and a plurality of column lines crossing the plurality of row lines. A pixel is formed at respective crossings of the row and column lines. Each pixel generates a charge based on light incident thereon and selectively transfers the charge to an associated column line based on a signal received from an associated row line. Each column line has a column driver circuit associated therewith. The column driver circuit is configured to generate an output voltage based on the charge on the associated column line.

[0014] For example, the pixel may include a transfer transistor for transferring the charge produced by a photo diode to an associated column line.

[0015] In another exemplary embodiment, the image sensor includes a plurality of row lines and a plurality of column lines crossing the plurality of row lines. A pixel is formed at respective crossings of the row and column lines. Each pixel generates a charge based on light incident thereon and selectively transfers the charge to an associated column line based on a

signal received from an associated row line. Each column line has a reset circuit associated therewith. Each reset circuit is configured to reset the charge of each pixel associated with the associated column line.

[0016] For example, a reset circuit may include a transistor for applying a supply voltage to the associated column line.

[0017] In an exemplary embodiment of the image sensing method of the present invention, voltages are applied to the column lines based on the charges generated by in the pixels. Then, for each column line, a data voltage is generated as an output voltage based on the applied voltage.

[0018] In one exemplary embodiment, prior to the applying step, the charge of each pixel is reset.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the accompanying drawings, in which:

[0020] FIG. 1 illustrates an example of a prior art CMOS image sensor having a photo diode and four transistor structure;

[0021] FIG. 2 is a circuit diagram showing pixels and column driver circuit of a CMOS image sensor according to a first exemplary embodiment of the present invention;

[0022] FIG. 3 is a flow chart showing a CMOS image sensing method

using the CMOS image sensor of FIG. 2;

[0023] FIG. 4 is a timing diagram showing the operation of the CMOS image sensor of FIG. 2;

[0024] FIG. 5 is a circuit diagram showing a column driver circuit of a CMOS image sensor according to a second exemplary embodiment of the present invention; and

[0025] FIG. 6 is a timing diagram showing the operation of the CMOS image sensor of FIG. 5.

DESCRIPTION OF EMBODIMENTS

[0026] Detailed illustrative embodiments of the present invention are disclosed herein. However, specific structural and functional details disclosed herein are merely representative for purposes of describing exemplary embodiments of the present invention. This invention may, however, be embodied in many alternate forms and should not be construed as limited to the embodiments set forth herein.

[0027] Accordingly, while the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that there is no intent to limit the invention to the particular forms disclosed, but on the contrary, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention. Like numbers refer to like elements throughout

the description of the figures.

<Embodiment 1>

[0028] FIG. 2 is a circuit diagram showing pixels and a column driver circuit of a CMOS image sensor according to a first exemplary embodiment of the present invention.

[0029] Referring to FIG. 2, a plurality of row lines 215 and a plurality of column lines 213 define a matrix and a pixel 200 is located at respective crossings of the row and column lines 215 and 213. Each of the pixels 200 comprises a photoelectric transformation element 203 and a switching element 205. For example, the photoelectric transformation element 203 has a photo diode or a photo gate light sensitive region. In the photo gate light sensitive regions, a photo gate electrode is disposed over the photo diode so that the charge signal (or photo charge) accumulated at the photo diode may be transmitted to a sensing node 201, which in this embodiment is on the associated column line 213. Namely, the sensing node 201 stores the charge signal generated by the photo diode while a data voltage is detected, and generates a voltage signal corresponding to the stored charges. As described in detail below, the charges accumulated at the sensing node 210 are discharged during a reset operation.

[0030] The switching element 205 may be an NMOS transistor or a PMOS transistor. The switching element 205 may be a depletion mode MOSFET (Metal Oxide Silicon Field Effect Transistor) or an enhancement mode

MOSFET. A conductive channel is formed under a gate electrode (or a control electrode) of the depletion mode MOSFET. The depletion mode MOSFET already has the conductive channel through which current may flow between a source electrode and a drain electrode of the depletion mode MOSFET, and thus the charge signal is easily transferred to the sensing node 201.

[0031] The depletion mode MOSFET 205 is referred to as a transfer transistor since the charge signal generated from the photo diode is transferred to the sensing node 201 by the depletion mode MOSFET 205.

[0032] A gate electrode of the transfer transistor 205 is connected to a row line 215, a source electrode of the transfer transistor 205 is connected to an anode of the photo diode, and a drain electrode of the transfer transistor 205 is connected to the sensing node 201.

[0033] As further shown in FIG. 2, each of the column lines 213 includes a column driver circuit 210. Each column driver circuit 210 includes a reset control circuit 207, a driver circuit 209 and an output load 211. The reset control circuit 207 performs a reset operation by discharging charges of the sensing nodes 201. The driver circuit 209 is controlled by the voltage level at the sensing nodes 201, and outputs one of a reference voltage and a data voltage based on the voltage level of the sensing nodes 201. Hereinafter, the reference voltage is referred to as an output voltage of the pixel when the reset control circuit 207 is turned on, and the data voltage is referred to as an output voltage of the pixel when the reset control circuit

207 is turned off and the transfer transistor 205 is turned on. The output load 211 is coupled to an output terminal of the driver circuit 209, and maintains the output of the driver circuit 209 above a given voltage level.

[0034] The reset control circuit 207 may include a reset transistor. For example, as shown in FIG. 2, the reset transistor 207 comprises a depletion mode NMOS transistor. A drain electrode of the reset transistor 207 is coupled to a power or supply voltage Vdd, and a source electrode of the reset transistor 207 is coupled to a column line 213. The reset transistor 207 is turned on or turned off in response to a reset control signal Rs received at a gate electrode of the reset transistor 207.

[0035] The driver circuit 209 may include a driver transistor. For example, the driver transistor 209 is an enhancement mode NMOS transistor. A drain electrode of the driver transistor 209 is coupled to the power voltage Vdd, and a source electrode of the driver transistor 209 is connected to the output load 211. A gate electrode of the driver transistor 209 is connected to the column line 213, and is controlled by the voltage level of the column line 213. The driver transistor 209 operates in a saturation region as a source follower amplifier during a reset operation or when the transfer transistor 205 is turned on.

[0036] The output load 211 may include a bias transistor. For example, as shown in FIG. 2, the bias transistor 211 is an enhancement mode NMOS transistor. A source electrode of the bias transistor 211 is connected to a ground, and a drain electrode of the bias transistor 211 is connected to the

source electrode of the drive transistor 209. The gate of the bias transistor 211 receives a bias Vbias. The bias transistor 211 acts as a constant current source and as an output transistor of a current mirror (not shown) when the bias transistor 211 operates in the saturation region. Thus, the bias transistor 211 acts as an active load.

[0037] The voltage of the source electrode of the driver transistor 209 is an output of the column driver circuit 210. The output of the column driver circuit 210 is sampled by a correlated double sampling circuit CDS (not shown).

[0038] FIG. 3 is a flow chart showing a CMOS image sensing method using the CMOS image sensor of FIG. 2, and FIG. 4 is a timing diagram showing the operation of the CMOS image sensor of FIG. 2.

[0039] Referring to FIGS. 3 and 4, when a reset control signal Rs has a high level, the reset transistor 207 in each column driver circuit 210 is turned on and a reset operation begins. Since the drain electrode of the reset transistor 207 has the voltage level of the power voltage Vdd, a voltage difference is formed between the source and drain electrodes of the reset transistor 207 when electrons remain at the sensing node 201. Thus, the electrons remaining at the sensing node 201 are attracted toward the drain electrode of the reset transistor 207 via the conductive channel. The electrons remaining at the sensing node 201 are discharged toward the power voltage (Vdd) source, and the voltage level of the sensing node 201 has substantially the same level as that of the power voltage Vdd.

[0040] The above reset operation is simultaneously performed on each of the pixels of the CMOS image sensor (step S10).

[0041] The driver transistor 209 operates in a saturation region because the voltage level of the sensing node 201 is about Vdd. In order that the driver transistor 209 may operate in the saturation region, Vgs of the driver transistor 209 needs to be higher than a threshold voltage (Vth) of the driver transistor 209 and Vgd of the driver transistor 209 needs to be lower than the threshold voltage (Vth) of the driver transistor 209 when the driver transistor 209 is an enhancement mode MOSFET.

[0042] As a result of the reset operation, the driver transistor 209 outputs the reference voltage (step S20).

[0043] The bias transistor 211 acts as a constant current source. In order that the driver transistor 209 may supply a constant current, Vgs' of the bias transistor 211 is determined based on the condition in which $Ids = K(Vgs' - Vth)^2$, wherein Ids is the drain-source current of the driver transistor 209. The bias transistor 211 operates in the saturation region, and the output voltage of the pixel is set at a given DC level. Thus, the reference voltage is Vdd – Vgs, and the reference voltage is input to a correlated double sampling circuit CDS.

[0044] Each of the column lines 213 is coupled to a correlated double sampling circuit CDS. The correlated double sampling circuit CDS samples the reference voltage and the data voltage, and outputs the difference between the reference voltage and the data voltage. In other words, an

output of the correlated double sampling circuit equals the difference between the reference voltage and the data voltage.

[0045] When the reset transistor 207 is turned off and light is applied to a photo diode 203, electron-hole pairs (EHPs) are generated. The photo diode 203 has a PN junction, and a depletion area is formed at the PN junction. The electrons recombine with the holes in the depletion area and disappear. An N type semiconductor has a plurality of positive ions, and a P type semiconductor has a plurality of negative ions, thus the potential of the N type semiconductor is higher than the potential of the P type semiconductor in the depletion area. As a result, an electric field is formed from the N type semiconductor to the P type semiconductor in the depletion area. The electrons of the EHPs generated from the P type semiconductor are attracted toward the N type semiconductor to be accumulated at the N type semiconductor by the electric field formed in the depletion area of the PN junction.

[0046] When a row line selection signal Tg has a high level, the transfer transistors 205 connected thereto are turned on. The charges generated by the photo diodes 203 associated with these transfer transistors 205 are transferred to the respective sensing nodes 201 via the transfer transistors 205 (step S30). Since the sensing nodes 201 have the voltage level of the power voltage Vdd because of the reset operation, there is formed a voltage difference between the source and drain electrodes of each transfer transistor 205 that is turned on. Thus, the electrons accumulated at the

source electrodes of the transfer transistors 205 are attracted toward the drain electrodes of the transfer transistors 205. The potential of the drain electrodes (or the sensing nodes 201) of the transfer transistors 205 decreases due to the movement of the electrons.

[0047] The potential of the gate electrode of a driver transistor 209 decreases according to above described process, and the potential decrease of the gate electrode of the driver transistor 209 is reflected at the output of the driver transistor 209 since the driver transistor 209 acts as the source follower amplifier in the saturation region.

[0048] Since the small signal voltage gain of the source follower amplifier is about 1, the voltage variation of the gate electrode of the driver transistor 209 is substantially the same as the voltage variation of the source electrode of the driver transistor 209. Thus, the potential decrease of the gate electrode of the driver transistor 209 leads to a potential decrease of the source electrode of the driver transistor 209, and the potential decrease of the source electrode of the driver transistor 209 is input as the data voltage to a correlated double sampling circuit. Namely, the data voltage is sampled by the correlated double sampling circuit (step S40). Since the correlated double sampling circuit outputs the voltage difference between the reference voltage and the data voltage, the resulting image data corresponds to the difference between the reference voltage and the data voltage.

[0049] An image signal sensed by the photo diode 203 may be represented

by the variations in the difference between the reference voltage and the data voltage. In order to enhance the sensitivity of the image sensor, the variations in the difference between the reference voltage and the data voltage are increased and the driver transistor 209 is operated in the saturation region. That is, the voltage level of the sensing node 201 (or the gate electrode of the driver transistor 209) is higher than the threshold voltage Vth of the driver transistor 209 before application of the selection signal T_{g+1} for the next row line.

[0050] When a small amount of light is incident on the photo diode 203, the amount of the generated EHPs is small. Thus, the voltage variation at the gate electrode of the driver transistor 209 is small, and the difference between the reference voltage and the data voltage is small. When a large amount of light is incident on the photo diode 203, the amount of the generated EHPs is large, and the difference between the reference voltage and the data voltage is large.

[0051] After the image sensing operation is performed on a row line, the image sensing operation is performed on a next row line. Thus, the signal Rs has a high level and the reset operation is performed before application of the selection signal T_{g+1} for the next row line. In an example embodiment, the reset signal Rs is a periodic signal, and therefore the reset operation is performed periodically on each pixel of the image sensor.

<Embodiment 2>

[0052] FIG. 5 is a circuit diagram showing a column driver circuit 210′ of a CMOS image sensor according to a second exemplary embodiment of the present invention.

[0053] Referring to FIG. 5, the configuration of the CMOS image sensor is the same as that of the CMOS image sensor of FIG. 2, however, the column driver circuit 210′ of this embodiment further includes a selection control circuit 217 that controls the output of the driver circuit 209 by turning on/off the driver circuit 209 . The selection control circuit 217 includes a starting transistor. For example, the starting transistor 217 is an enhancement mode NMOS transistor. A drain electrode of the starting transistor 217 is connected to a source electrode of the driver transistor 209, and a source electrode of the starting transistor 217 is connected to the output load (or the bias transistor 211). In addition, an output terminal of the column driver circuit 210′ is the source electrode of the starting transistor 217. The gate of the starting transistor 217 receives a start signal Vstart.

[0054] The start signal Vstart is applied such that the starting transistor 217 remains in a turned-on state during the reset operation, and such that the starting transistor 217 remains in the turned-on state when the data voltage is being output after the reset operation. The start signal Vstart is applied such that the starting transistor 217 is turned off when the output of the data voltage and sampling of the data voltage by the correlated double sampling circuit are complete, and to initialize the output voltage of the

column driver circuit 210'.

[0055] FIG. 6 is a timing diagram showing the operation of the CMOS image sensor of FIG. 5.

[0056] Referring to FIG. 6, when the reset signal Rs becomes a high level after the starting transistor 217 is turned on, the reset transistor 207 is turned on. As described in detail in Embodiment 1, the sensing node 201 of each pixel 200 is reset, and the voltages of the sensing nodes 201 become the power voltage Vdd.

[0057] The voltage of sensing node 201 is output as the reference voltage via the associated driver transistor 209 and the starting transistor 217 of the column driver circuit 201'. The starting transistor 217 operates in a triode region in order that the reference voltage may be output. Namely, the channel area approximate to a drain region of the starting transistor 217 is not in pinch-off.

[0058] In addition, since the driver transistor 209 and the bias transistor 211 operate in the saturation region, the size of the starting transistor 217 is relatively large in order that the current flowing through the driver transistor 209 and the bias transistor 211 in the saturation region may be substantially the same as the current flowing through the starting transistor 217 in the triode region. In other words, the area of the source/drain region of the starting transistor 217 is larger than that of the driver transistor 209 and the bias transistor 211.

[0059] The transfer transistors 205 of the pixels 200 connected to the (i)th

row line are turned on in order to select the pixels connected to the (i)th row line.

[0060] The data voltages are output according to the transfer transistors 205 being turned on as described in Embodiment 1.

[0061] The starting transistors 217 remain in the turned-on state while the data voltages are output.

[0062] The respective correlated double sampling circuits (not shown) sample the data voltages while the data voltages are output. The image sensing for the pixels connected to the (i)th row line ends when the starting transistors 217 are turned off. The starting transistors 217 are turned off when gate electrodes of the starting transistors 217 have a low voltage level, and the signal path between the output terminal of the column driver circuits CDSs and the column lines 213 of the image sensor are disconnected. The operation region of the bias transistors 211 varies from the saturation region to the triode region because of the disconnection of the signal path, and the charges accumulated at the capacitors of the correlated double sampling circuits are discharged to the ground via the channel of bias transistors 211.

[0063] Thus, the output voltage of a column driver circuit is about 0 volt when the associated starting transistor 217 is turned off, so that the output signal of the column driver circuit CDS is initialized.

[0064] Then, the starting transistors 217 are turned on again so as to perform the image sensing operation for the pixels connected to (i+1)th row

line, and the image sensing operation is performed on the pixels connected to (i+1)th row line according to above mentioned procedure.

[0065] While the exemplary embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations may be made herein without departing from the scope of the invention.